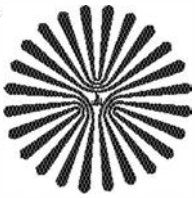

PNU University

Advanced Analog Integrated Circuits Design

Dr. Hamed Aminzadeh

امروزه کتاب‌خوانی و علم‌آموزی، نه تنها یک وظیفه ملی، که یک واجب دینی است.[1]

مقام معظم رهبری

در عصر حاضر یکی از شاخصه‌های ارزیابی رشد، توسعه و پیشرفت فرهنگی هر کشوری میزان تولید کتاب، مطالعه و کتاب‌خوانی مردم آن مرز و بوم است. ایران اسلامی نیز از دیرباز تاکنون با داشتن تمدنی چندهزارساله و مراکز متعدد علمی، فرهنگی، کتابخانه‌های معتبر، علما و دانشمندان بزرگ با آثار ارزشمند تاریخی، سرآمد دولت‌ها و ملت‌های دیگر بوده و در عرصه فرهنگ و تمدن جهانی به‌سان خورشیدی تابناک همچنان می‌درخشد و با فرزندان نیک‌نهاد خویش هنرنمایی می‌کند. چه کسی است که در دنیا با دانشمندان فرزانه و نام‌آور ایرانی همچون ابوعلی سینا، ابوریحان بیرونی، فارابی، خوارزمی و ... همچنین شاعران برجسته‌ای نظیر فردوسی، سعدی، مولوی، حافظ و ... آشنا نباشد و در مقابل عظمت آنها سر تعظیم فرود نیاورد. تمامی این افتخارات ارزشمند، برگرفته از میزان عشق و علاقه فراوان ملت ما به فراگیری علم و دانش از طریق خواندن و مطالعه منابع و کتاب‌های گوناگون است. به شکرانه الهی، تاریخ و گذشته ما، همیشه درخشان و پربار است. ولی اکنون در این زمینه در چه جایگاهی قرار داریم؟ آمار و ارقام ارائه‌شده از سوی مجامع و سازمان‌های فرهنگی در مورد سرانه مطالعه هر ایرانی، برایمان چندان امیدوارکننده نمی‌باشد.

کتاب، دروازه‌ای به سوی گستره دانش و معرفت است و کتاب خوب، یکی از بهترین ابزارهای کمال بشری است. همه دستاوردهای بشر در سراسر عمر جهان، تا آنجا که قابل کتابت بوده است، در میان دست‌نوشته‌هایی است که انسان‌ها پدید آورده و می‌آورند. در این مجموعه بی‌نظیر، تعالیم الهی، درس‌های پیامبران به بشر، و همچنین علوم مختلفی است که سعادت بشر بدون آگاهی از آن‌ها امکان‌پذیر نیست. کسی که با دنیای زیبا و زندگی‌بخش کتاب ارتباط ندارد بی‌شک از مهم‌ترین دستاورد انسانی و نیز از بیشترین معارف الهی و بشری محروم است. با این دیدگاه، به‌روشنی می‌توان ارزش و مفهوم رمزی عمیق در این حقیقت تاریخی را دریافت که اولین خطاب خداوند متعال به پیامبر گرامی اسلام(ص) این است که »بخوان!« و در اولین

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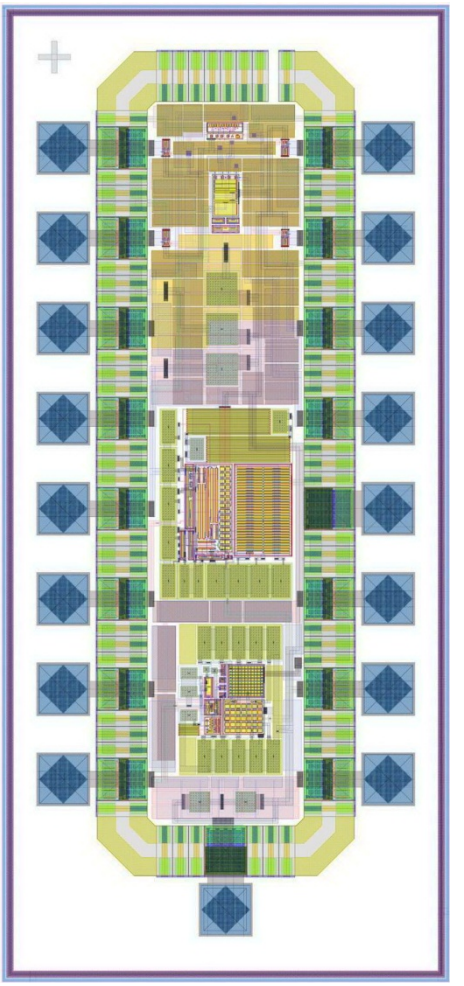
۱. پیام مقام معظم رهبری به مناسبت آغاز هفته کتاب ۷۲/۱۰/۴

سوره‌ای که بر آن فرستاده عظیم‌الشأن خداوند، فرود آمده، نام «قلم» به تجلیل یاد شده‌است: «إِقْرَأْ وَ رَبُّکَ الْاَکْرَمُ. اَلَّذی عَلَّمَ بِالْقَلَم» در اهمیت عنصر کتاب برای تکامل جامعه انسانی، همین بس که تمامی ادیان آسمانی و رجال بزرگ تاریخ بشری، از طریق کتاب جاودانه مانده‌اند.

دانشگاه پیام‌نور با گستره جغرافیایی ایران‌شمول خود با هدف آموزش برای همه، همه‌جا و همه‌وقت، به‌عنوان دانشگاهی کتاب‌محور در نظام آموزش عالی کشورمان، افتخار دارد جایگاه اندیشه‌سازی و خردورزی بخش عظیمی از جوانان جویای علم این مرز و بوم باشد. تلاش فراوانی در ایام طولانی فعالیت این دانشگاه انجام پذیرفته تا با بهره‌گیری از تجربه‌های گرانقدر استادان و صاحب‌نظران برجسته کشورمان، کتاب‌ها و منابع آموزشی درسی شاخص و خودآموز تولید شود. در آینده هم، این مهم با هدف ارتقای سطح علمی، روزآمدی و توجه بیشتر به نیازهای مخاطبان دانشگاه پیام‌نور با جدیت ادامه خواهد داشت. به‌طور قطع استفاده از نظرات استادان، صاحب‌نظران و دانشجویان محترم، ما را در انجام این وظیفه مهم و خطیر یاری‌رسان خواهد بود. پیشاپیش از تمامی عزیزانی که با نقد، تصحیح و پیشنهادهای خود ما را در انجام این وظیفه خطیر یاری می‌رسانند، سپاسگزاری می‌نماییم. لازم است از تمامی اندیشمندانی که تاکنون دانشگاه پیام‌نور را منزلگه اندیشه‌سازی خود دانسته و ما را در تولید کتاب و محتوای آموزشی درسی یاری نموده‌اند، صمیمانه قدردانی گردد. موفقیت و بهروزی تمامی دانشجویان و دانش‌پژوهان عزیز آرزوی همیشگی ما است.

دانشگاه پیام‌نور

Contents



Two analog integrated circuits (a bandgap reference and an operational amplifier) designed and embedded in a monolithic chip: Submitted at June 2020 by Dr. Hamed Aminzadeh and Mohammad Mahdi Valinezhad for fabrication in 0.18µm CMOS technology.

Preface

The field of analog integrated circuit is embraced by CMOS technology over the recent years, offering cost-effective and highly efficient approaches for dominating the microelectronics market. Despite bipolar and GaAs devices still find fruitful applications in electronics products, it is only the CMOS technology which offers viable and reliable solutions for the integration of advanced analog and mixed-signal microsystems. With the device channel dimension continuing to scale down to 0.05 μm and below, integrated MOS devices will continue to facilitate circuit design for the next several years. Analog circuit design technique has progressed with the CMOS process as well. High-power, high-voltage analog circuits with few transistors and capable of processing simple continuous-time analog signals have been substituted by low-power, low-voltage microsystems comprising thousands of MOS devices and various capabilities, including processing of large, discrete-time signals with high efficiency. As a result, many analog design techniques that were proved to be effective only a decade ago have been abandoned since they were not useful for present low-voltage analog circuits.

This book deals with the design and analysis of advanced analog integrated CMOS circuits, emphasizing on fundamentals and novel paradigms that the designer should master in today's electronics industry. Analog design requires both insight and intuition. Therefore, each concept in this book is introduced firstly from a basic perspective

and treated by careful analysis. The objective is to develop by intuition a solid foundation of analog circuit design and analysis so that the designer can learn the trade-offs between speed, area, power consumption, and the final error of each configuration. This approach enables the designer to apply the concepts of simple analog circuits to advanced circuits. The material of this book was taught firstly in the form of the presentation slides, enabling the writer to modify the format, order, and the contents of each chapter thoroughly. At first, we recognized what the reader should learn at each chapter, and then started to convey the most important concepts in simple and clear language. We gradually add the necessary modifications to arrive at the most advanced concepts proposed by the author in the literature. This procedure is particularly useful for learning analog circuits, since it allows the reader to pursue the evolution of a circuit and to learn both circuit analysis and synthesis simultaneously.

The context contains five chapters, whose context is selected carefully to provide the most important materials for self-study and classroom adoption in a semester. For each chapter at the beginning, we cover only a minimum of precise analysis, leaving the advanced concepts of the prior art to the rest of the chapter. First-time readers may not simply comprehend the advanced circuit design techniques before they study the principles of basic reference books. Therefore, an investigation on the primitive concepts is taught before starting to study the advanced models and configurations.

It is assumed that the reader is familiar with the basic techniques of circuit design and analysis. The book is therefore a complementary material for the elementary reference books, with an emphasis on the new achievements proposed by the author. Chapter 1 discusses briefly the fundamentals of the EKV model for the MOS devices. The EKV model finds its roots in the first transistor models, accounting for the weak, moderate and strong inversion regions together. Unlike the standard square-law model that fails to quantify the operating region and the behavior of the nano-scale transistors, the EKV model proves

to be accurate in relating the region of operation to the bias currents and bias voltages. The EKV model parameters are not, however, provided by many fabrication companies, yielding unknown variables in the design expressions. Chapter 2 introduces a systematic yet empirical transistor model relying on the g_m/I_D methodology. The most important advantage of the g_m/I_D methodology is that it can be evaluated through experimental or simulation procedures. This minimizes the gap between the accurate results of simulation and those of the analysis, enabling to predict with high accuracy the MOS transistor characteristics based on pre-computed lookup tables. After understanding the most important MOS device models in Chapters 1 and 2, Chapters 3 through 5 deal with more advanced topics: Integrated voltage references and voltage regulators, and integrated oscillators. These important subjects are very essential for an analog designer and can be found in the most analog, digital and mixed-signal microsystems.

This book follows the common notations used for the variables according to IEEE standard. An analog signal is composed of the sum of DC and small-signal quantities. An input voltage v_{IN}, for example, is the sum of the DC V_{IN} component and the incremental AC v_{in}.

In the end, the author would like to acknowledge the contribution of Mr. Mohammad Jamali for preparing a general draft of the chapters according to the teaching slides.

Dr. Hamed Aminzadeh,
Payame-Noor University
Summer 2020

List of Abbreviations

Common symbols and abbreviations are organized below by meaning.

A: Ampere, unit of current
AC: Alternating current
BGR: Bandgap Reference
BJT: Bipolar Junction Transistor
BSIM: Berkeley short-channel, insulated gate, FET model
BW: Bandwidth
CAD: Computer-aided design
CMOS: Complementary metal–oxide semiconductor
CMRR: Common-mode rejection ratio
CP: Charge pump
CS: Common-source
CSIM: Compact Short-Channel IGFET Model
CTAT: Complementary-to-absolute-temperature
DC: Direct current
DTC: Dead Time Control
EKV: Enz–Krummenacher–Vittoz MOS model
ESR: Equivalent Series Resistance
F: Farad, unit of capacitance
FET: Field effect transistor
FO: Fan-out
IC: Integrated circuit
JFET: Junction FET
K: Kelvin, (absolute) unit of temperature
KCL: Kirchhoff's Current Law
KVL: Kirchhoff's Voltage Law
GA: Genetic algorithm
GBW: Gain-bandwidth product
GM: Gain margin
Hz: Hertz, unit of frequency
ICA: Imperialist competitive algorithm
LDO: Low-dropout regulator
LDVS: Low-dropout voltage source
LHP: Left half-plane
MI: Moderate inversion
MOS: Metal–oxide semiconductor
MOSCAP: MOS capacitor

MOSFET: Metal–oxide semiconductor field-effect transistor
***n*MOS:** n-type metal–oxide semiconductor
NSGA: non-dominated sorting GA
OTA: Operational transconductance amplifier
Opamp: Operational Amplifier
PCDM: Parallel-compensated-depletion-mode
PM: Phase margin
***p*MOS:** p-type metal–oxide semiconductor
PSD: Power spectral density
PSRR: Power-supply rejection ratio
PTAT: Proportional-to-absolute-temperature
PVT: Process, voltage and temperature
PWM: Pulse-width-modulation
RFID: Radio-frequency identification
RHP: Right half-plane
RMS: Root mean square
SA: Simulated annealing
SCDM: Series-compensated-depletion-mode
SI: Strong inversion
SPICE: Stanford Program for Integrated Circuit Emulation
SR: Switching regulator; Slew rate
TC: Temperature coefficient
TSMC: Taiwan Semiconductor Manufacturing Company
UGF: Unity-gain frequency
V: Volt, unit of voltage
VCO: Voltage-controlled oscillators
VLSI: Very Large Scale Integration
W: Watt, unit of power
WI: Weak inversion
ZTC: Zero-temperature-coefficient

Chapter 1

EKV Model for MOS devices

1.1. Introduction

Modern large-scale integrated circuits are comprised inevitably of several MOS transistors and their interconnections. The first requirement of circuit design and analysis is the access to a reliable model for operation of the MOS transistors.

For analysis of the low-speed digital circuits, a very simple model may be more than sufficient, since every transistor serving in the logic circuits is operating similar to an on–off switch. As soon as fast transitions appear in the time domain of the switches activity, the model should be revised to describe the dynamic behavior of a logic circuit and to obtain the rise and fall time of the pulses. The same dynamic behavior happens when the frequency of a digital circuit approaches to the very high frequencies. More details must be added with the reduction of the power supply, including the residual current of the ‘off’ devices which plays an important role in the overall power consumption of the modern analog and digital circuits. Advanced electronics market is relied largely on the integrated complementary MOS (CMOS) circuits with the analog and digital sections operating together. Design of high-performance CMOS circuits requires an accurate model of the MOSFETs.

This chapter explains the basic motivations for developing the MOS transistor models that can be utilized for the design of CMOS circuits. It gives a short overview of the EKV transistor model,

motivated by the design and analysis of CMOS amplifiers based on the explained model. The EKV model is the result of a large body of work performed by C. C. Enz, F. Krummenacher, and E. A. Vittoz. The model not only describes the physics of the MOS transistors, but also provides the required tools for a circuit designer. The result is a precise and reliable model, which can predict correctly the voltages and currents of a four-terminal symmetric MOSFET, has smooth behavior with no discontinuity in the operating regions, and can measure the small-signal parameters.

1.2. Different Operating Regimes for MOS Devices

It is critical to understand the different regions of operation of a MOSFET as a prerequisite to design and analyze CMOS circuit. In this section, we apply the most important concepts of the MOS devices to quantify the operation of an *n*MOS implemented in a *p*-substrate [1]. The concepts of this section can be applied to describe the operation of the *p*MOS devices in a similar manner. Fig. 1.1 illustrates the possible operating regimes for a typical *n*-channel metal oxide semiconductor (*n*MOS). From the perspective of the gate–source voltage (V_{GS}), the operation of a MOSFET can be characterized

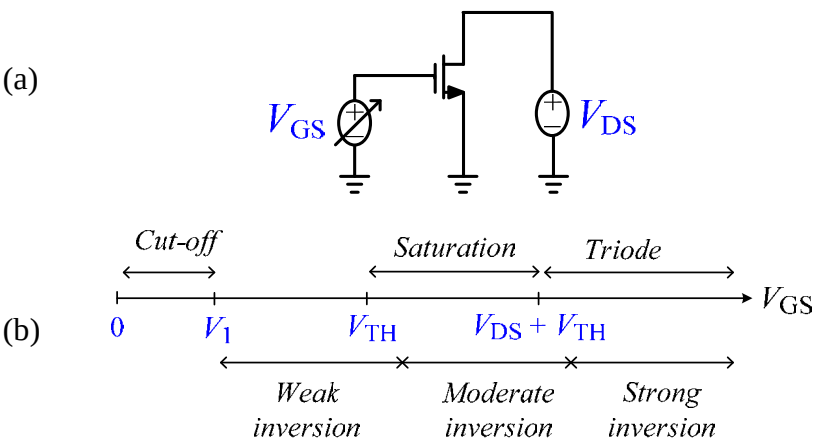


Fig. 1.1. The different operating regimes for an *n*MOS transistor.

by three operating regions [2, 3]:

1. Weak inversion (WI) for $V_{\mathrm{GS}} - V_{\mathrm{TH}} < 50$ mV,
2. Moderate inversion (MI) for $50\ \mathrm{mV} < V_{\mathrm{GS}} - V_{\mathrm{TH}} < 150\ \mathrm{mV}$,
3. Strong Inversion (SI) for $V_{\mathrm{GS}} - V_{\mathrm{TH}} > 150$ mV,

where V_{TH} is the threshold voltage.

From the perspective of the drain–source voltage, the possible operating regions are:

1. Triode: $V_{\mathrm{DS}} < V_{\mathrm{DS,sat}}$,
2. Saturation: $V_{\mathrm{DS}} > V_{\mathrm{DS,sat}}$,

where $V_{\mathrm{DS,sat}}$ is the saturation voltage and is equal to the overdrive voltage (V_{OV}) of the square-law model [3]. The overdrive voltage is:

$$V_{\mathrm{OV}} = V_{\mathrm{GS}} - V_{\mathrm{TH}}. \tag{1.1}$$

Calculation of DC biasing point is a first step towards circuit design and analysis. Common challenges are determining the drain current and the proper network that can fix the device operating point before performing small-signal analysis. In the case of a long-channel *n*MOS, the square-law model for the three widely-used regions of operation are [2-4]:

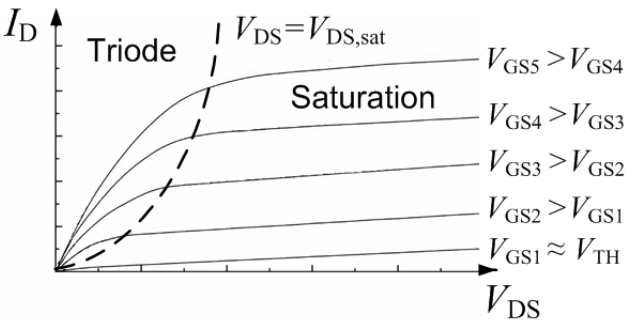
$$I_{\mathrm{D}} = \begin{cases} \left(\frac{W}{L}\right) I_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{N V_{\mathrm{T}}}\right)\left[1 - \exp\left(-\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right] & \text{WI} \\ \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right)(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2(1 + \lambda V_{\mathrm{DS}}) & \text{SI Saturation} \\ \mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right)\left[(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - \frac{1}{2}V_{\mathrm{DS}}^2\right] & \text{SI Triode} \end{cases} \tag{1.2}$$

where, W and L are the gate width and length, respectively, I_0 is the technology-dependent "technology current", μ is the carrier mobility, λ is the channel length modulation coefficient, and N is the sub-threshold slope factor. The thermal voltage (V_{T}) is defined as

$$V_{\mathrm{T}} = \frac{kT}{q} \approx 26\ \mathrm{mV}, \tag{1.3}$$

where, q is the charge of electron, k is the Boltzmann constant, and T is the absolute temperature. Fig. 1.2 determines the regions of operation of a MOSFET, revealing that the common square-law model fails to describe the MOS operating regimes and, most importantly, its operation at moderate inversion.

(a)



(b)

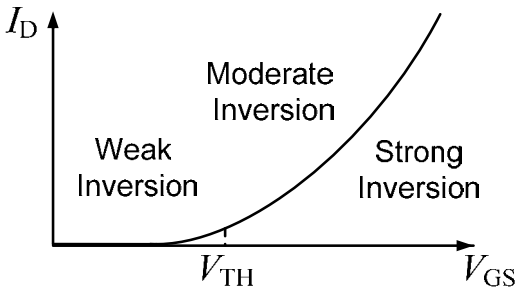


Fig. 1.2. Possible operating regions of a MOSFET from the perspectives of gate-source and drain-source voltages.

1.2.1. The traditional (Square-law) MOS Transistor Model for Different Regions

For our analysis of a MOS device operating at strong inversion, we initially assume that the transistor switches off abruptly as V_{GS} drops below V_{TH} [3]. In reality, for V_{GS}~V_{TH}, a "weak" inversion layer appears below the gate terminal and causes conduction from the drain terminal to the source (Fig. 1.3). Even for $V_{GS} < V_{TH}$, I_D is still finite, exhibiting an exponential dependence on V_{GS} that is known as "subthreshold conduction". Such dependence can be formulated as:

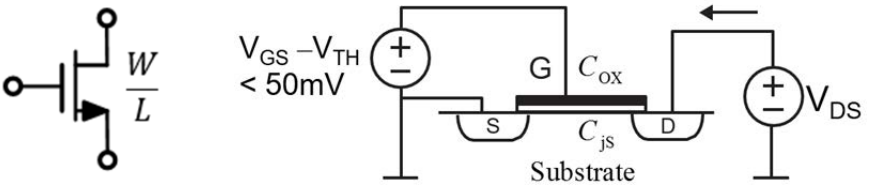


Fig. 1.3. Sub-threshold conduction of a MOSFET.

$$I_{\mathrm{D}} = \left(\frac{W}{L}\right) I_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{NV_{\mathrm{T}}}\right)\left[1 - \exp\left(-\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right], \qquad (1.4)$$

where, $N \geq 1$ is the sub-threshold slope factor that is expressed by:

$$N = 1 + \frac{C_{\mathrm{OX}}}{C_{\mathrm{jS}}}. \qquad (1.5)$$

In (1.5), C_{OX} is the gate capacitance per unit area and C_{jS} is the equivalent capacitance of the substrate. Referring to (1.4), the drain current grows exponentially with V_{GS} and $-V_{\mathrm{DS}}$. Therefore, the current becomes independent of V_{DS} for $V_{\mathrm{DS}} > 4V_{\mathrm{T}}$ (~100 mV), leading to the simpler drain current relationship shown below:

$$I_{\mathrm{D}} \approx I_{\mathrm{S}} \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{NV_{\mathrm{T}}}\right), \qquad (1.6)$$

where, $I_{\mathrm{S}} = (W/L)I_0$ is known as the 'specific current'. If a MOS device can still conduct for $V_{\mathrm{GS}} < V_{\mathrm{TH}}$, then how can we define the threshold voltage appeared in the above expressions? A few definitions have been proposed for the threshold voltage to date, one of which is to extrapolate the weak and strong inversion characteristics on a logarithmic vertical scale, and to define their intercept point as V_{TH}.

The exponential dependence of I_{D} upon V_{GS} suggests the usage of subthreshold MOS devices for achieving higher transconductances similar to the bipolar devices. However, since subthreshold conduction appears for large devices biased by low drain current, the speed of the subthreshold devices is mostly compromised in the weak

inversion. Increasing the gate-source voltage to higher than the threshold voltage drives the transistor into strong inversion, where the following expression exists for operation at strong-inversion saturation by ignoring the channel length modulation:

$$I_{\mathrm{D}} \approx \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right)(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{\mathrm{W}}{\mathrm{L}}\right) {V_{\mathrm{OV}}}^2. \quad (1.7)$$

Table 1.1 shows the traditional algebraic expressions used to model the different operating regions of a MOSFET. The small-signal transconductance (g_{m}) is defined as the change in the drain current divided by the change in the gate-source voltage ($g_{\mathrm{m}} = \partial I_{\mathrm{D}}/\partial V_{\mathrm{GS}}$) [5]. This parameter is presented in Table 1.1 for different regions.

The designer should analyze each region separately, using the specific equation proposed for the corresponding region. The main weakness of the model is that no voltage/current expression can describe the device operation in moderate inversion regime.

Table 1.1 Traditional (Square-Law) Model for Different Regions

Operating Region	Current	Transconductance
Weak Inversion (Triode or Saturation)	$I_{\mathrm{D}} = \left(\frac{W}{L}\right) I_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{NV_{\mathrm{T}}}\right) \left[1 - \exp\left(-\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right]$	$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} \approx \frac{I_{\mathrm{D}}}{NV_{\mathrm{T}}}$
Strong Inversion (Saturation)	$I_{\mathrm{D}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right) (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 (1 + \lambda_{\mathrm{n}} V_{\mathrm{DS}})$	$g_{\mathrm{m}} \approx \sqrt{2\mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right) \times I_{\mathrm{D}}}$
Strong Inversion (Triode)	$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right) \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{1}{2} V_{\mathrm{DS}}^2\right]$	$g_{\mathrm{m}} \approx \mu_{\mathrm{n}} C_{\mathrm{OX}} \left(\frac{W}{L}\right) V_{\mathrm{DS}}$

1.2.2. Transit Frequency

A very common way to characterize the high-frequency behavior of a MOSFET is to look at the frequency at which the small-signal current gain of a common-source amplifier falls to unity. The measurement of the current gain is presented in Fig. 1.4(a), which can be found by dividing the small-signal drain current (i_d) to the gate current (i_g). The transit frequency (f_T) is defined as the frequency where $i_d/i_g = 1$. It is a key parameter for characterizing the bandwidth of the most analog circuits.

Consider the small-signal equivalent circuit of the schematic of Fig. 1.4(a) in Fig. 1.4(b), where the drain and source terminals are tied together and shorted to ground. The small-signal gate-source voltage (v_{gs}) can be related to the gate current as:

$$v_{gs}(s) = \frac{i_g(s)}{s(C_{GS} + C_{GD})}, \tag{1.8}$$

where, C_{GS} and C_{GD} are the gate-source and gate-drain capacitors, respectively. Since $i_d(s) = g_m v_{gs}(s)$, we conclude that:

$$i_d(s) \approx i_g(s) \frac{g_m}{s(C_{GS} + C_{GD})} \Rightarrow \frac{i_d(s)}{i_g(s)} \approx \frac{g_m}{s(C_{GS} + C_{GD})}. \tag{1.9}$$

Under the steady-state conditions, we set $s = j\omega$, and f_T can be measured as (1.10):

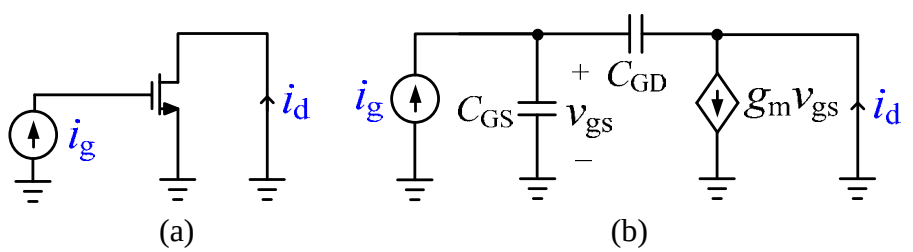


Fig. 1.4. (a) Main circuit and (b) the small-signal equivalent circuit for evaluating the transit frequency.